

April 1993

Features

- 64 Analog Switches in an 8 x 8 x 1 Array
- On-Chip Line Decoder and Control Latches
- Automatic Power-Up Reset by Using a 0.1 μ F Capacitor at the MR Pin
- R_{ON} Resisted 95 Ω at $V_{CC} = 4.5V$
- Analog Signal Capability: $V_{DD}/2$
- Wide Operating Temp. Range: -40°C to +85°C

Family Features

- CD74HC Types
 - 2V to 10V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{DD} ; at $V_{DD} = 5V$ and 10V
- CD74HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility: $V_{IL} = 0.8V$ Max, $V_{IH} = 2V$ Min
 - CMOS Input Compatibility: $I_I < 1\mu A$ at V_{OL} , V_{OH}

Description

The CD74HC22106 and CD74HCT22106 are digitally controlled analog switches which utilize silicon-gate CMOS technology. The CD74HC22106 type features CMOS input-voltage-level compatibility and the CD74HCT22106 features LSTTL input-voltage-level compatibility.

The Master Reset has an internal pull-up resistor and is normally used with a 0.1 μ F capacitor. During power up all switches are automatically reset. The crosspoint switches will reset with MR = 0 even if CE is high. A 6-bit address through a 6 line to 64 line decoder selects the transmission gate which can be turned on by applying a logical ONE to the DATA input and logical ZERO to the STROBE. Similarly, any transmission gate can be turned OFF by applying a logical ZERO to the DATA input while strobing the STROBE with a logical ZERO.

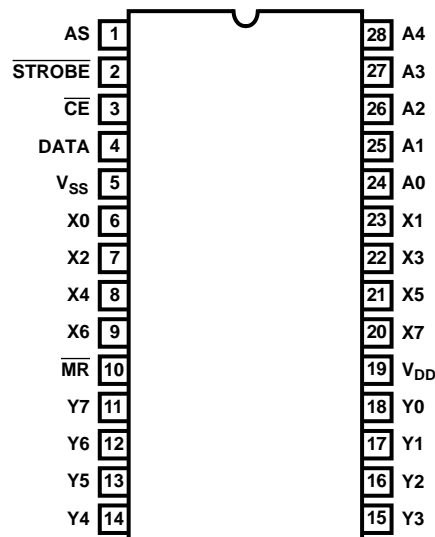
The CE pin allows the crosspoint array to be cascaded for matrix expansion in both the X and Y directions.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CD74HC22106E	-40°C to +85°C	28 Lead Plastic DIP
CD74HCT22106E	-40°C to +85°C	28 Lead Plastic DIP

Pinout

CD74HC22106, CD74HCT22106
(PDIP)
TOP VIEW



Specifications CD74HC22106, CD74HCT22106

Absolute Maximum Ratings

DC Supply Voltage (V_{DD})
 Voltage Reference to V_{SS} Terminal. -0.5V to +11V
 DC Input Diode Current
 I_{IK} (for $V_I < -0.5$ or $V_I > V_{DD} + 0.5V$) $\pm 20mA$
 DC Output Diode Current
 I_{OK} (For $V_O < -0.5$ or $V_O > V_{DD} + 0.5V$) $\pm 20mA$
 DC Transmission Gate Current $\pm 25mA$
 Power Dissipation per Package (P_D)
 For $T_A = -40^\circ C$ to $+60^\circ C$ (Package Type E). 500mW
 For $T_A = -60^\circ C$ to $+85^\circ C$ (Package Type E). Derate Linearly at
 12mW/ $^\circ C$ to 200mW
 Junction Temperature $+175^\circ C$
 Junction Temperature (Plastic Package) $+150^\circ C$
 Lead Temperature (Soldering 10 Sec.) $+300^\circ C$

Operating Conditions

Operating Temperature Range (T_A)
 Package Type E $-40^\circ C$ to $+85^\circ C$
 Storage Temperature Range $-65^\circ C \leq T_A \leq +150^\circ C$
 Supply Voltage Range (for $T_A =$ Full Package Temp. Range) V_{DD}
 CD74HC22106 2V to 10V
 CD74HCT22106 4.5V to 5.5V
 DC Input or Output Voltage V_I, V_O 0V to V_{DD}

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications $V_{SS} = GND$

PARAMETERS	CD74HC22106							CD74HCT22106							UNITS	
	TEST CONDITIONS		+25°C			-40°C to +85°C		TEST CONDITIONS		+25°C			-40°C to +85°C			
	V_{IS} (V)	V_{DD} (V)	MIN	TYP	MAX	MIN	MAX	V_{IS} (V)	V_{DD} (V)	MIN	TYP	MAX	MIN	MAX		
High-Level Input Voltage V_{IH}	-	2	1.5	-	-	1.5	-	-	4.5 to 5.5	2	-	-	2	-	V	
	-	4.5	3.15	-	-	3.5	-	-								
	-	9	6.3	-	-	6.3	-	-								
Low-Level Input Voltage V_{IL}	-	2	-	-	0.5	-	0.5	-	4.5 to 5.5	-	-	0.8	-	0.8	V	
	-	4.5	-	-	1.35	-	1.35	-								
	-	9	-	-	2.7	-	2.7	-								
Input Leakage Current (Any Control) I_L	V_{DD} or GND	10	-	-	± 0.1	-	± 1	Any Voltage Between V_{DD} & GND	5.5	-	-	± 0.1	-	± 1	μA	
Quiescent Device Current, I_{CC} (with MR = 1)	V_{DD} or GND	10	-	-	5	-	50	V_{DD} or GND	5.5	-	-	2	-	20	μA	
Off Leakage Current, I_L (with MR = 1)	All Switches OFF	10	-	-	0.1	-	1	-	5.5	-	-	0.1	-	1	μA	
"On" Resistance R_{ON}	V_{DD} to GND Figures 8, 9	2	-	470	700	-	875	Figure 8	4.5	-	64	95	-	120	Ω	
		4.5	-	64	95	-	120									
		9	-	45	70	-	90									
	$V_{DD}/2$	-	-	-	-	-	-	-	-	4.5	-	58	85	-	110	Ω
		4.5	-	58	85	-	110									
		9	-	40	60	-	80									
"On" Resistance Between Any Two Channels ΔR_{ON}	V_{DD} to GND	-	-	-	-	-	-	V_{DD} to GND	4.5	-	25	-	-	-	Ω	
		4.5	-	25	-	-	-									
		9	-	23	-	-	-									

Specifications CD74HC22106, CD74HCT22106

Dynamic Electrical Specifications $V_{SS} = 0V$

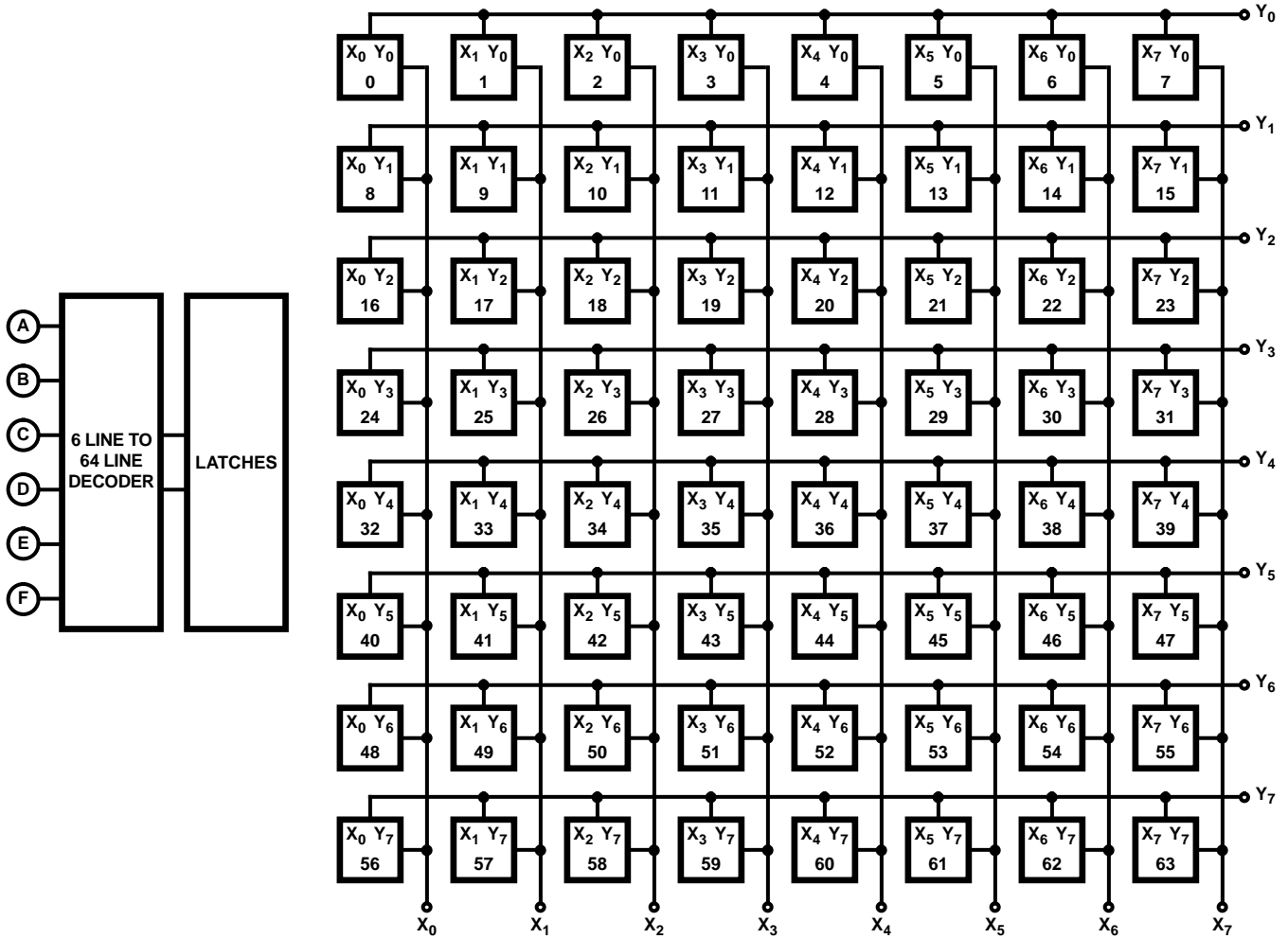
PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS										UNITS			
			+25°C					-40°C to +85°C								
			HC		HCT			HC		HCT						
			FIG.	V_{DD} (V)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX				
CONTROLS																
Propagation Delay Time:	t_{PZH}	$R_L = 10k\Omega$ $C_L = 50pF$ $t_R, t_F = 6ns$	1	2	-	370	-	-	-	385	-	-	ns			
Strobe to Output (Switch Turn-On to High Level)				4.5	-	110	-	120	-	125	-	135	ns			
				9	-	65	-	-	-	70	-	-	ns			
Data-In to Output (Turn-On to High Level)	t_{PZH}			2	2	-	240	-	-	-	255	-	-	ns		
					4.5	-	75	-	85	-	85	-	95	ns		
					9	-	50	-	-	-	55	-	-	ns		
Address to Output (Turn-On to High Level)	t_{PZH}				3	2	-	380	-	-	-	400	-	-	ns	
						4.5	-	110	-	120	-	125	-	135	ns	
						9	-	65	-	-	-	75	-	-	ns	
Propagation Delay Time:	t_{PHZ}				1	2	-	400	-	-	-	420	-	-	ns	
Strobe to Output						4.5	-	135	-	150	-	155	-	170	ns	
						9	-	90	-	-	-	100	-	-	ns	
Data-In to Output (Turn-On to Low Level)	t_{PZL}				2	2	-	240	-	-	-	255	-	-	ns	
						4.5	-	75	-	85	-	85	-	95	ns	
						9	-	50	-	-	-	55	-	-	ns	
Address to Output (Turn-Off)	t_{PHZ}				3	2	-	420	-	-	-	440	-	-	ns	
						4.5	-	140	-	150	-	155	-	170	ns	
						9	-	95	-	-	-	100	-	-	ns	
Minimum Set-Up Time (Data-In to Strobe Address)	t_{SU}				-	2	35	-	-	-	40	-	-	-	ns	
						4.5	20	-	20	-	20	-	20	-	-	ns
						9	15	-	-	-	15	-	-	-	-	ns
Minimum Hold Time (Data-In to Strobe Address)	t_H				-	2	85	-	-	-	90	-	-	-	ns	
						4.5	25	-	25	-	25	-	25	-	-	ns
						9	20	-	-	-	20	-	-	-	-	ns
Minimum Strobe Pulse Width	t_W				-	2	200	-	-	-	210	-	-	-	ns	
						4.5	45	-	55	-	55	-	65	-	-	ns
						9	25	-	-	-	30	-	-	-	-	ns
Maximum Switching Frequency	F_O				-	2	0.7	-	-	-	0.6	-	-	-	MHz	
						4.5	3.0	-	2.8	-	2.8	-	2.6	-	-	MHz
						9	7	-	-	-	6.5	-	-	-	-	MHz
Input (Control) Capacitance	C_I				-	-	-	10	-	10	-	10	-	10	pF	

Specifications CD74HC22106, CD74HCT22106

Dynamic Electrical Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	V _{IS} (V _{P-P})	V _{SS} (V)	V _{DD} (V)	LIMITS								UNITS
						+25°C				-40°C to +85°C				
						HC		HCT		HC		HCT		
						MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Propagation Delay Time, Signal Input to Output	t _{PLH} , t _{PHL}	R _L = 10kΩ C _L = 50pF t _R , t _F = 6ns	-	0	2	-	30	-	-	-	33	-	-	ns
			-	0	4.5	-	20	-	20	-	22	-	22	ns
			-	-	9	-	15	-	-	-	17	-	-	ns
						HC Typical		HCT Typical						
Switch Frequency Response at -3dB	f _{3dB}	R _S = R _L = 600Ω	2	-2.25	2.25	5	5	-	-	-	-	-	-	MHz
			2	-4.5	4.5	6	6	-	-	-	-	-	-	MHz
Crosstalk Between Any Two Channels	F _{CT}	R _S = R _L = 600Ω f = 1kHz	2	-2.25	2.25	-110	-110	-	-	-	-	-	-	dB
			2	-2.25	2.25	-53	-53	-	-	-	-	-	-	dB
		R _S = R _L = 600Ω f = 1MHz	2	-2.25	2.25	-53	-53	-	-	-	-	-	-	dB
			2	-4.5	4.5	-55	-55	-	-	-	-	-	-	dB
Switch "OFF" -40dB Feed Through Frequency	F _{DT}	R _S = R _L = 600Ω	2	-2.25	2.25	7	7	-	-	-	-	-	-	MHz
			2	-4.5	4.5	8	8	-	-	-	-	-	-	MHz
Total Harmonic Distortion	THD	R _L = 10kΩ f = 1kHz sine-wave	4	-2.25	2.25	0.05	0.05	-	-	-	-	-	-	%
			8	-4.5	4.5	0.05	0.05	-	-	-	-	-	-	%
		R _L = 600Ω f = 1kHz sine-wave	4	-2.25	2.25	0.25	0.25	-	-	-	-	-	-	%
			7	-4.5	4.5	0.12	0.12	-	-	-	-	-	-	%
Control to Switch Feed-Through Noise (DATA IN, Strobe, Address)		R _L = 10kΩ t _R , t _F = 6ns	V _{DD}	0	5	35	35	-	-	-	-	-	-	mV
			V _{DD}	0	10	65	65	-	-	-	-	-	-	mV
Capacitance, Xn to GND	C _{IS}	f = 1MHz	-	0	10	48	48	-	-	-	-	-	-	pF
			-	0	10	44	44	-	-	-	-	-	-	pF

Functional Diagram



CD74HC22106, CD74HCT22106

TRUTH TABLE

A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	SWITCH SELECT	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	SWITCH SELECT
0	0	0	0	0	0	X ₀ Y ₀	1	0	0	0	0	0	X ₀ Y ₄
0	0	0	0	0	1	X ₁ Y ₀	1	0	0	0	0	1	X ₁ Y ₄
0	0	0	0	1	0	X ₂ Y ₀	1	0	0	0	1	0	X ₂ Y ₄
0	0	0	0	1	1	X ₃ Y ₀	1	0	0	0	1	1	X ₃ Y ₄
0	0	0	1	0	0	X ₄ Y ₀	1	0	0	1	0	0	X ₄ Y ₄
0	0	0	1	0	1	X ₅ Y ₀	1	0	0	1	0	1	X ₅ Y ₄
0	0	0	1	1	0	X ₆ Y ₀	1	0	0	1	1	0	X ₆ Y ₄
0	0	0	1	1	1	X ₇ Y ₀	1	0	0	1	1	1	X ₇ Y ₄
0	0	1	0	0	0	X ₀ Y ₁	1	0	1	0	0	0	X ₀ Y ₅
0	0	1	0	0	1	X ₁ Y ₁	1	0	1	0	0	1	X ₁ Y ₅
0	0	1	0	1	0	X ₂ Y ₁	1	0	1	0	1	0	X ₂ Y ₅
0	0	1	0	1	1	X ₃ Y ₁	1	0	1	0	1	1	X ₃ Y ₅
0	0	1	1	0	0	X ₄ Y ₁	1	0	1	1	0	0	X ₄ Y ₅
0	0	1	1	0	1	X ₅ Y ₁	1	0	1	1	0	1	X ₅ Y ₅
0	0	1	1	1	0	X ₆ Y ₁	1	0	1	1	1	0	X ₆ Y ₅
0	0	1	1	1	1	X ₇ Y ₁	1	0	1	1	1	1	X ₇ Y ₅
0	1	0	0	0	0	X ₀ Y ₂	1	1	0	0	0	0	X ₀ Y ₆
0	1	0	0	0	1	X ₁ Y ₂	1	1	0	0	0	1	X ₁ Y ₆
0	1	0	0	1	0	X ₂ Y ₂	1	1	0	0	1	0	X ₂ Y ₆
0	1	0	0	1	1	X ₃ Y ₂	1	1	0	0	1	1	X ₃ Y ₆
0	1	0	1	0	0	X ₄ Y ₂	1	1	0	1	0	0	X ₄ Y ₆
0	1	0	1	0	1	X ₅ Y ₂	1	1	0	1	0	1	X ₅ Y ₆
0	1	0	1	1	0	X ₆ Y ₂	1	1	0	1	1	0	X ₆ Y ₆
0	1	0	1	1	1	X ₇ Y ₂	1	1	0	1	1	1	X ₇ Y ₆
0	1	1	0	0	0	X ₀ Y ₃	1	1	1	0	0	0	X ₀ Y ₇
0	1	1	0	0	1	X ₁ Y ₃	1	1	1	0	0	1	X ₁ Y ₇
0	1	1	0	1	0	X ₂ Y ₃	1	1	1	0	1	0	X ₂ Y ₇
0	1	1	0	1	1	X ₃ Y ₃	1	1	1	0	1	1	X ₃ Y ₇
0	1	1	1	0	0	X ₄ Y ₃	1	1	1	1	0	0	X ₄ Y ₇
0	1	1	1	0	1	X ₅ Y ₃	1	1	1	1	0	1	X ₅ Y ₇
0	1	1	1	1	0	X ₆ Y ₃	1	1	1	1	1	0	X ₆ Y ₇
0	1	1	1	1	1	X ₇ Y ₃	1	1	1	1	1	1	X ₇ Y ₇

Test Circuits and Waveforms

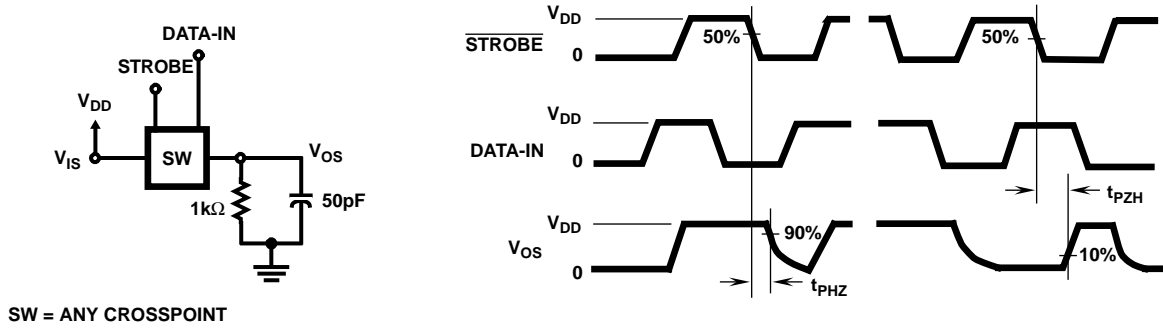


FIGURE 1. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

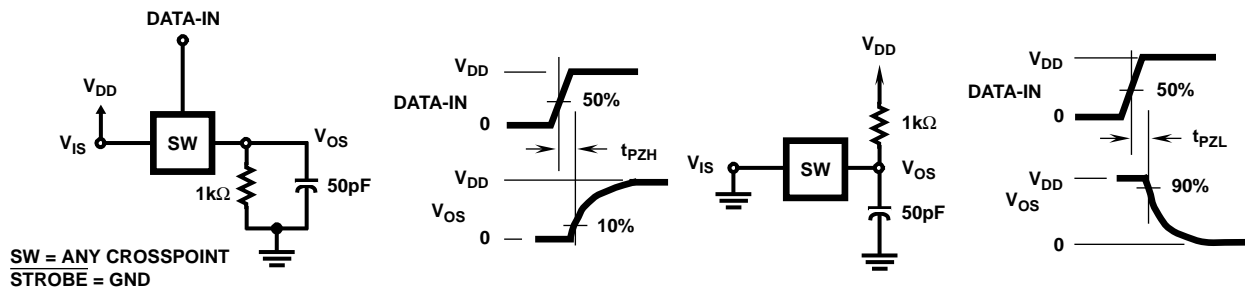


FIGURE 2. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (DATA-IN TO SIGNAL OUTPUT, SWITCH TURN-ON TO HIGH OR LOW LEVEL)

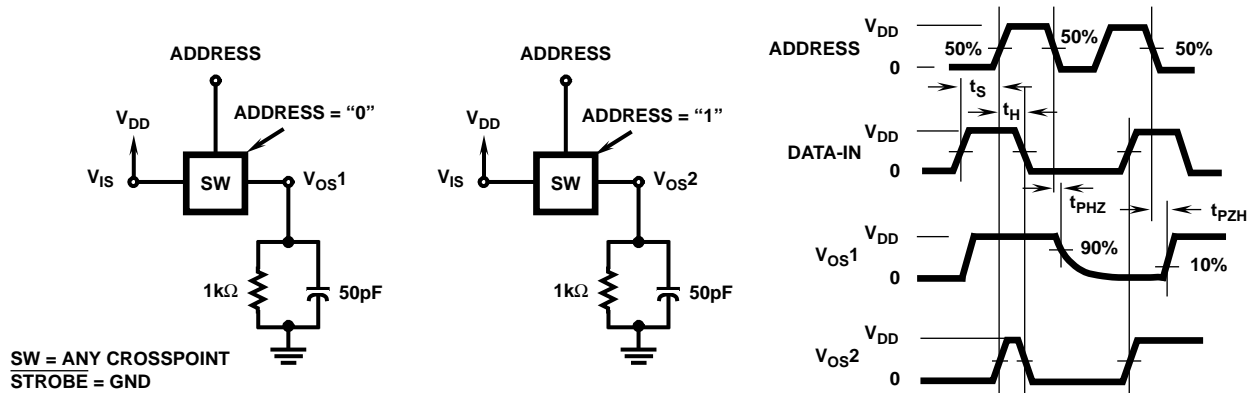


FIGURE 3. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (ADDRESS TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

Typical Application Information

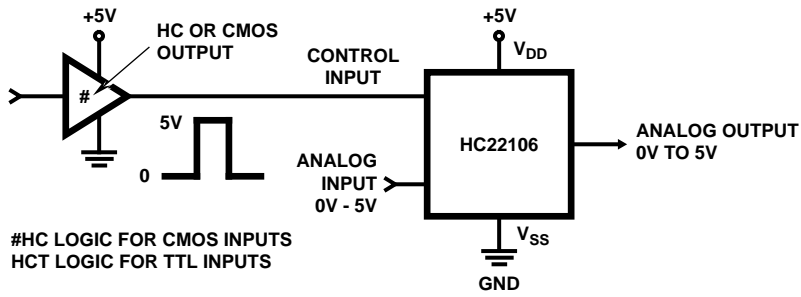


FIGURE 4. TYPICAL SINGLE SUPPLY CONNECTION FOR HC22106

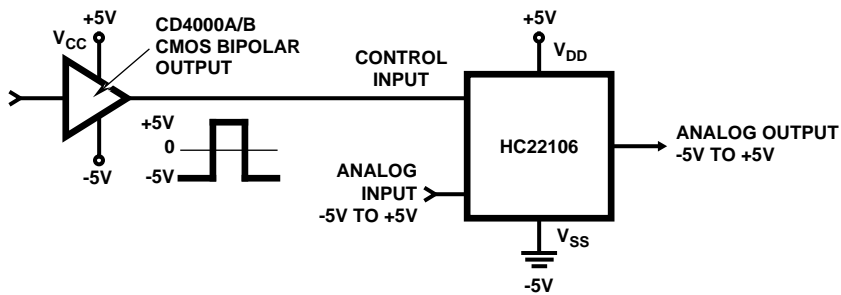


FIGURE 5. TYPICAL DUAL SUPPLY CONNECTION FOR HC22106

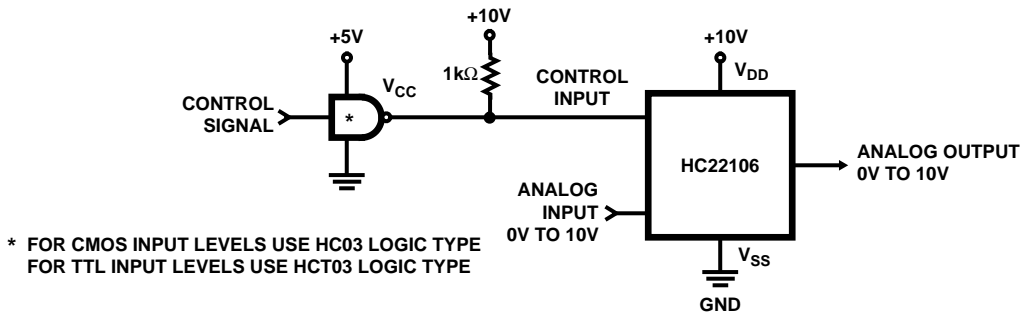


FIGURE 6. USE OF HC/HCT03 WHEN CONTROL IS 0V - 5V AND ANALOG SIGNAL IS 0V - 10V

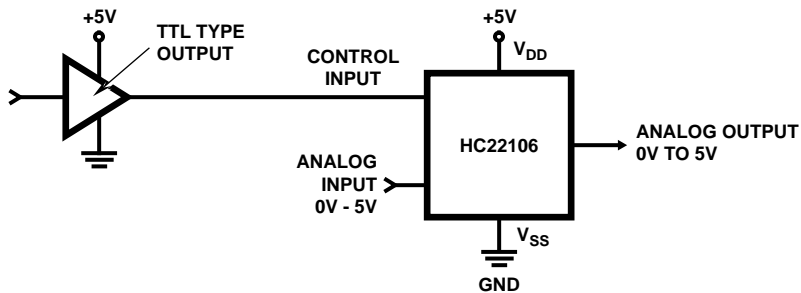


FIGURE 7. TYPICAL SINGLE SUPPLY CONNECTION FOR HCT22106 WITH TTL INPUT

Typical Performance Curves

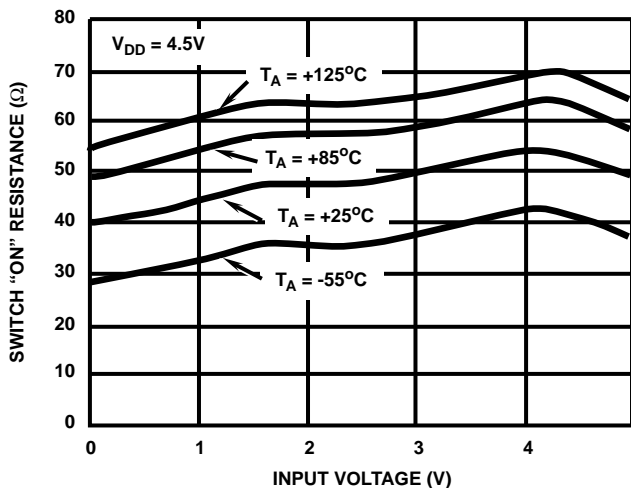


FIGURE 8. TYPICAL "ON" RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE vs TEMPERATURE

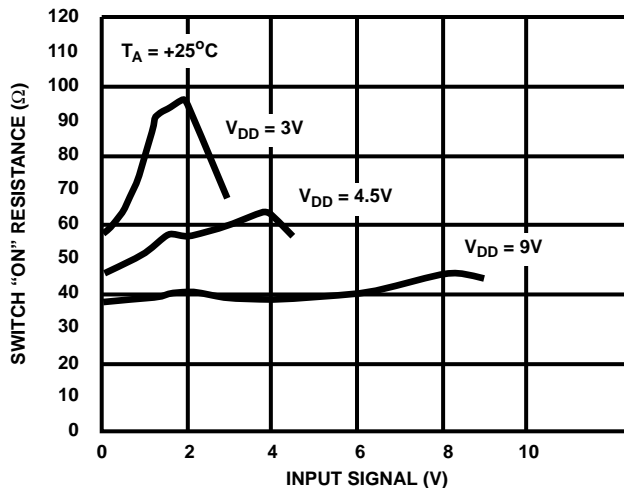


FIGURE 9. TYPICAL "ON" RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE vs V_{DD}

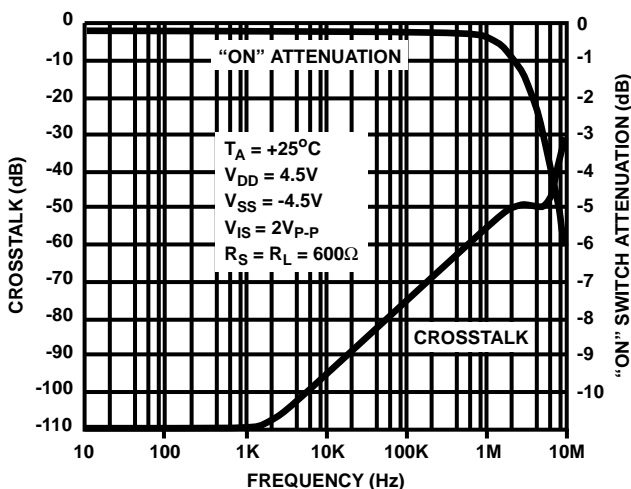


FIGURE 10. TYPICAL "ON" SWITCH ATTENUATION AND CROSSTALK AS A FUNCTION OF FREQUENCY

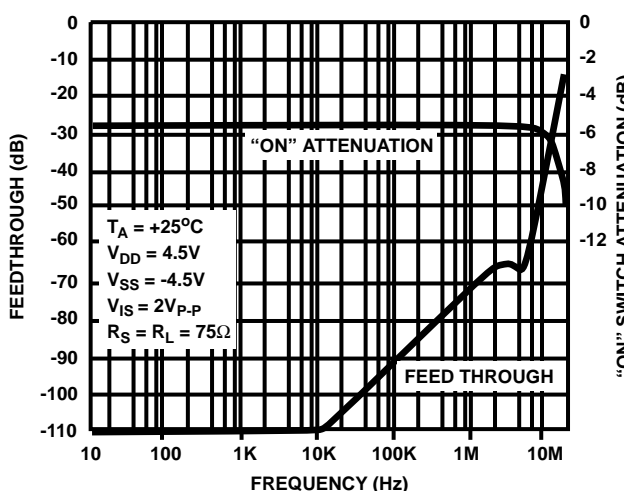


FIGURE 11. TYPICAL "ON" SWITCH ATTENUATION AND "OFF" SWITCH FEED THROUGH AS A FUNCTION OF FREQUENCY